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1. SCOPE

This document describes the operation of the Mk IV Pattern Recognition Detector, (herein referred to as 'Rack P') and its intended capabilities and limitations.

2. RELEVANT DOCUMENTS

PS 3002-101-30/2	Opacity Pattern Recognition Theory of Operation
PS 3006-101-31	Rack 'P' System Generation and Operation
PS 3006-102-12	Rack 'P' to Mk IV Head Interface Specification
PS 3006-101-12	Special Detector Interface Specification

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3. GENERAL DESCRIPTION

- 3.1 The interrogation head consists of a white light source channelled through fibre optic guides, which illuminates a strip of the note as it passes the head.

Light reflected from the note surface is collected in fibre optic guides, and channelled to 32 photo-detectors. Each detector receives light reflected from an area of note approximately 7 mm x 4 mm.

- 3.2 Signals from the detectors are amplified and multiplexed onto a line to the Data Acquisition Board in Rack 'P' mounted externally to the 3400. The multiplex address is transmitted to the head from that board.

It is arranged that only the outputs from detectors covering the expected note area are sampled. These are selected by Rack 'P' CPU according to the note dimensions and expected lateral position. The required detector outputs are sampled sequentially by the Data Acquisition hardware on command from the CPU.

Samples are made at 4 mm intervals as the note passes the head, but the first and last 2 mm are not scanned.

- 3.3 Data received and converted by the Data Acquisition Board is normally passed directly to the comparison hardware which consists of one or more Correlation Boards.

The boards are initialised by the CPU prior to each note reaching the detector, and operate independently from the processor while receiving data.

Each Correlation Board contains permanently stored reference data obtained from a sample of each type of note to be recognised, and receives the same data from the Data Acquisition board. The data received is combined with the data stored according to an arithmetic expression as defined in PS 3002-101-30/2. At the note end, the processor reads the results contained in each board, and calculates correlation coefficients for each pattern.

If the highest coefficient exceeds a pre-defined value and the difference between itself and the next highest coefficient exceeds a second pre-defined value, the note is classified as the pattern corresponding to the highest coefficient. If the coefficient fails the tests, the note is deemed 'unclassified'.

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3.4 Under test conditions, the output of the Data Acquisition Board can be read directly by the CPU. In this way, data from samples of notes to be recognised can be obtained. (See Specification No PS 3006-101-39 for procedure).

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4. SYSTEM FACILITIES

4.1 Note Recognition

4.1.1 Up to 64 patterns may be used at any time. Normally each note type requires 4 patterns since notes may be presented in any orientation. The code returned to Rack 'D' is the complete pattern number, ie including the orientation information. It is possible to configure the system such that orientation data is inappropriate, in which case these bits may have an alternative meaning.

It is intended that the number of patterns available in the future be extended to 96.

4.1.2 All patterns used at any one time must relate to notes of nominally the same dimensions, notes of different sizes being sorted in separate passes. Patterns for these notes can be stored in the system and selected by process code. This allows 64 'live' patterns for each process. The maximum number of processes possible depends on the note sizes - typically, data for 6 different processes can be stored.

4.1.3 Limitations

- (i) The correlation coefficient is reduced if notes are dirty, damaged, or presented out of position, but it is expected that the best match will remain correct. The pass threshold is therefore selected to give an acceptable unclassified rate.
- (ii) If a note is presented which does not in fact have a corresponding pattern in the system, the best match coefficient cannot be guaranteed to fall below the pass threshold.

4.2 Test Facilities

4.2.1 The following information is available via a printer connected to the CPU board (P3): (Messages will only be printed when the printer is connected, when the rack is powered up or on reset).

- (i) On power-up or reset, the first Test is to check the RAM. If this is faulty the LED on the 101M processor card will flash with an equal mark/space ratio.

The PROM contents are then validated against a checksum. If this proves faulty, the LED will remain on, indicating an EPROM fault.

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S1 (on the 101M card), is next interrogated. If this is OFF, the 'P' rack will continue through further tests (below), and if a fully functioning system is found the machine will be ready to use.

If S1 is ON, the 'P' rack will be set up to permanently scan. This will enable the engineer to test out head, to Buffer Multiplexer, to Data Acquisition signals. The LED will flash with a mark/space ratio of 5:1 to show that it is in the 'scan' mode.

- (ii) On power-up or reset, and on receipt of the process code, the CPU checks the status of the hardware. Any fault found causes an error code message to be printed. (See Specification No PS 3006-101-39).

4.2.2 The following information is available via a printer connected to the CPU board (P3):

If, on receipt of a process code, which is identical to a previous process code sent, the following information will be printed out:- (the printer having been connected on the last power up or CPU reset).

Note: In order to send a process code the same as the previous code, this is done every time the screen is 'refreshed' ie OPERATORS FUNCTION 18.

```
CURRENT PROCESS CODE XXXXXXXX
CURRENT DELAY (NOM = 6) Y
CURRENT PASS VALUE %A
CURRENT DIFF VALUE %B
```

CODE	QTY	LOW	HIGH	AVERAGE
0	F	G	H	I
2	F	G	H	I
3	F	G	H	I
etc				
NOTREC	J			

Where:-

- X = Current process code P rack is running in.
- Y = The delay being used at present (see para. 5.7).
- A = The current pass % that the maximum correlation figure must be greater than to be classified.
- B = The current difference % that the best and next best correlation differences must be greater than to be classified.
- F = The quantity of notes (for the particular code) that has been fed since the last process code was sent).
- G = The lowest correlation coefficient of the F notes fed.

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- H = The highest correlation coefficient of the F notes fed.
- I = The average correlation coefficients of the F notes fed.
- J = The number of notes that were not classified due to them not meeting the pass and difference figures for this process.

4.2.3 Calibration

The Data Acquisition Board requires matching to the detector head in use. This is achieved by means of a non-volatile memory which stores correction values for each channel. The values are obtained and programmed semi-automatically using the procedure described in Specification No. PS 3006-101-39. A printer connected to the CPU board records any errors detected during the calibration process.

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5. HARDWARE CONFIGURATION

5.1 A single pattern recognition system comprises the following circuit boards, housed in a TM990/520 8 slot chassis, with power supplies as detailed below.

- (i) TM990/101M (or equivalent) CPU board.
- (ii) 3409-5006 Clock/Memory Card.
- (iii) TM990/305 Parallel Interface Card.
- (iv) 3409-5075 Data Acquisition Card.
- (v) Up to four 3409-5076 Correlation Cards.

Ultimately, the number of Correlation Cards may be increased to six. This will entail use of a large chassis, and/or production of a combination Clock/Memory/Interface Card.

5.2 The system will normally be situated externally to the note transport (3400), and will connect to the MkIV head via a multi-twisted pair cable of 10 metres maximum length as defined in PS 3006-102-12.

5.3 Connection is also required to the External Detector Processor 'P', via a multi-twisted pair cable of 3 metres maximum length, as defined in PS 3006-101-12. This provides process information, synchronisation with the note transport and information concerning the relative position of each note prior to reaching the detector head.

5.4 The system requires a 180 to 250, (or 90 to 125) volt single phase, 47 to 63 Hz supply. Power consumption 200 watts maximum.

5.5 The system software is generated from 2/3 separate links:-

(i) Procedure

This is currently called PRCK0302 ie version 3, issue 2. This is situated in memory from 0 to >1FFF and is contained on the 101M CPU board:-

U44 >0000 to >FFE
U42 >0001 to >FFF
U45 >1000 to >1FFE
U43 >1001 to >1FFF

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A suitable link file is shown below:-

```

NOPAGE
TASK PRCK03NN           ;NN = current issue
PROGRAM 0
DATA >F000             ;start address of ram
COMMON >2000,PRCTBL    ;start address of
COMMON >1F80,CONTID,DIFCID,CLCKID,PDECID
COMMON PDECID,DACQID,CORRID,XOPSID,CKSMID
INCLUDE directory.OBJ.CONTO3NN
INCLUDE directory.OBJ.DIFCO3NN
INCLUDE directory.OBJ.CLCKO3NN
INCLUDE directory.OBJ.PDECO3NN
INCLUDE directory.OBJ.DACQO3NN
INCLUDE directory.OBJ.CORRO3NN
INCLUDE directory.OBJ.XOPSO3NN
INCLUDE directory.OBJ.CKSMO3NN
END

```

5.6 Interrupt links on the CLOCK MEMORY card in 'P' Rack:-

SK10 Link pins 9 to 18
Link pins 8 to 17

5.7 Delay Facility

With all software up to PRCK031C there has been a fixed delay present of 6 mm allowing the note to be in exactly the right position with reference to the head.

The facility has now been added so that this delay can be varied to optimise the suspect rate, this being done by S1 to S8 on the clock memory card within the 'P' Rack.

The switch settings are an offset from the nominal 6 mm. They are an inverted signed displacement S1 LSB and S8 MSB.

ie

S8	S7	S6	S5	S4	S3	S2	S1	Signed Disp.	Actual Delay
0	0	0	0	0	0	0	1	-2	4
0	0	0	0	0	0	0	0	-1	5
1	1	1	1	1	1	1	1	0	6 Nominal
1	1	1	1	1	1	1	0	+1	7
1	1	1	1	1	1	0	1	+2	8
etc									

The actual delay can be checked by connecting a printer to 'P' Rack, see para. 4.2.2.

NOTE: WHEN RECORDING ENSURE DELAY IS SET TO NOMINAL.

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